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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,012	12/23/2005	Hiroyuki Furushima	Q91175	2834

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EXAMINER	
PHAM, JOHN D	

ART UNIT	PAPER NUMBER
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,012	FURUSHIMA ET AL.	
	Examiner	Art Unit	
	JOHN D. PHAM	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *23 December, 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 are cancelled.

2. Claims 5-8 are presented for examination.

3. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP p 2100-8, c 2, l 45-48; p 2100-9, c 1, l 1-4). The Examiner has full latitude to interpret each claim in the broadest reasonable sense. The Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 23 December, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject

matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zifferer et al (US Pat. No. 5349518) in view of Beck et al (US Pub. No. 2002/0147505) further in view of Jungleib (US Pat. No. 5886274).

Referring to claim 5, Zifferer et al teach:

An apparatus comprising of an instruction table for correlatively storing instructions (Zifferer et al, column 7, lines 36-37, a database of records of instruction);

A search for parameter of the instruction (Zifferer et al, column 7, lines 16-24, address or location or symbol of instruction);

A storing unit for containing input/output address data as sequence program component (Zifferer et al, column 7, lines 32-36, database file wherein maintain cross reference for the address);

Zifferer et al fail to teach a component data creating means to create variable table data table by replacing input/output type with variable name.

However, Beck et al teach constructing a symbolic input-output type variable (Beck et al, paragraph [0014], line 5-7, each variable has an identification field) for automatically replacement of input/output symbolic variables with exact address.

Zifferer et al and Beck et al are analogous art because they are from methods of developing ladder logic program for Programmable Logic Controller (PLCs).

At the time of the invention, it would have been obvious for one of ordinary skill in the art, having the teaching of Zifferer et al and Back et al, to modify the ladder logic programming of Zifferer et al to include the table of symbolic variable of input/output object type of Beck et al because the modification will automatically replace the symbolic variables by constructing the exact input/output address of each symbolic variable.

The motivation of doing so would have been obvious because the programming an automation application capable of manipulating data exchange between an application and input/output modules in a symbolic form and allow the program to be written independently with the automation equipment (Beck et al, paragraph [0018], lines 3-8).

Therefore, it would have been obvious to combine Zifferer et al with Beck et al to obtain the invention as specified in claim 5.

As to claim 6, Zifferer et al teach:

A storing component for containing component data as sequence program component (Zifferer et al, column 2, lines 47-54, allocate storage space for components file);

A sequence component display device for displaying stored program component (Zifferer et al, column 3, lines 46-50, a list of predefined symbol display);

A sequence programming means for selecting desired sequence component (Zifferer et al, column 3, lines 48-56, Quick Search Option to select symbols from the predefined symbol list).

Regarding claims 5-6, the combined Zifferer et al/Beck et al teach a system and method for creating sequence program for programmable controller with automatic internal addresses replacement (Zifferer et al, column 3, lines 34-40) and automatic input/output addresses replacement (Beck et al, paragraph [0013], lines 3-6).

The combined Zifferer et al/Beck et al fail to teach the ladder editor can divert or copy and paste a portion of an existing sequence program into a new sequence program.

However, Jungleib teaches a sequencer editor preferably allow users to copy and paste a program sequence (Jungleib, column 7, lines 44-47).

The combined Zifferer et al/ Beck et al and Jungleib are analogous art because they are from method of ladder logic programming for Programmable Logic Controller.

At the time of the invention, it would have been obvious for one of ordinary skill in the art, having the teaching of the combined Zifferer et al/Beck et al and Jungleib, to modify the ladder programming editor system described by the combined Zifferer et al/Beck et al to include the feature copy and paste of Jungleib because the later ladder programming editor will allow user to modify of an infinite variety of input sequence program.

The motivation for doing so would have been obvious because user or programmer has the capability of modifying of an infinite variety of existing sequence program (Jungleib, column 2, lines 17-21).

Therefore, it would have been obvious to combine the Zifferer et al/Beck et al with Jungleib to obtain the invention as specified in claim 5-6.

Referring to claim 7, Zifferer et al teach:

A method of creating a sequence program comprising:

A search and discriminate step for input/output type parameter of the instruction (Zifferer et al, column 7, lines 16-24, a search step in two ways for symbols and for addresses);

A storing and creating step for storing search result table by combining the discriminated input/output type, with an address in the code in the selected portion of the sequence program (Zifferer et al column 7, lines 32-36, database file for maintain cross reference of addresses);

Zifferer et al fail to teach a component data creating step to create variable table data table by replacing input/output type with variable name.

However, Beck et al teach a step of constructing a symbolic input-output type variable (Beck et al, paragraph [0018], lines 1-5, each variable has an identification fields).

Zifferer et al and Beck et al are analogous art because they are from methods of developing ladder logic program for Programmable Logic Controller (PLCs).

At the time of the invention, it would have been obvious for one of ordinary skill in the art, having the teaching of Zifferer et al and Beck et al, to modify the method of ladder logic programming of Zifferer et al to include a step of constructing the table of symbolic variable of input/output object type of Beck et al because the modification will automatically replace the symbolic variables by constructing the exact input/output address of each symbolic variable.

The motivation of doing so would have been obvious because the method of programming an automation application can be capable of manipulating data exchange between an application and input/output modules in a symbolic form and allow the program to be written independently with the automation equipment (Beck et al, paragraph [0018], lines 3-8).

Therefore, it would have been obvious to combine Zifferer et al with Beck et al to obtain the invention as specified in claim 7.

As to claim 8, Zifferer et al teach:

A storing step for containing component data as sequence program component (Zifferer et al column 2, lines 49-54, allocate storage space for file);

A sequence component display step for displaying stored program component (Zifferer et al, column 3, lines 48-50);

A sequence programming selection step for selecting desired sequence component (Zifferer et al, column 3, lines 48-50, Quick Search option for select symbol from a predefined list).

Regarding claims 7-8, the combined Zifferer et al/Beck et al teach a method for creating sequence program for programmable controller with automatic internal addresses replacement (Zifferer et al, column 3, lines 34-40) and automatic input/output addresses replacement (Beck et al, paragraph [0013], lines 3-6, replace symbolic input/output variables).

The combined Zifferer et al/ Beck et al and Jungleib are analogous art because they are from method of ladder logic programming for Programmable Logic Controller.

At the time of the invention, it would have been obvious for one of ordinary skill in the art, having the teaching of the combined Zifferer et al/Beck et al and Jungleib, to add the copy and paste capability to the method of ladder programming described by the combined Zifferer et al/Beck et al to include a step of copy and paste of Jungleib because the later method of ladder programming will allow user to modify of an infinite variety of existing sequence program.

The motivation for doing so would have been obvious because user or controller logic programmer has the method of modifying of an infinite variety of existing sequence program (Jungleib, column 2, lines 17-21).

Therefore, it would have been obvious to combine the Zifferer et al/Beck et al with Jungleib to obtain the invention as specified in claim 7-8.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsui et al (US Pat No. 4455619) disclose a system to provide a programming method and programming equipment which makes possible sequence programming for attaining a desired processing function with ease and without substantial knowledge about the electronic computer, and which allow automatic symbol replacement.

Yamane et al (US Pat. No. 5717588) disclose a programming system (programmable controller) that has control factors, input/output addresses symbolic instructions and the like forming a sequence program are stored in a memory, and when an operator inputs a control factor prior to execution of the sequence program, information corresponding to the control factor stored in the memory is called and shown on a display, whereby debug of the sequence program is facilitated.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN D. PHAM whose telephone number is (571)270-1590. The examiner can normally be reached on Monday-Friday 8:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER
2/4/08